

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

- SUB B17
1. (Currently Amended) A subcode-data generating circuit, which generates subcode data including subcode component data which indicates ~~any~~ at least one of time information and information other than the time information, said circuit comprising:
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- a first generating portion for automatically generating the subcode component data which indicates the time information;
- a second generating portion for automatically generating the subcode component data which indicates the information other than the time information; and
- a selecting portion which selects an output of at least one of ~~the outputs of~~ said first and second generating portions.
2. (Original) The subcode-data generating circuit, as claimed in claim 1, wherein said second generating portion comprises a plurality of generating portions provided separately.
3. (Currently Amended) A subcode-data generating circuit, which generates subcode data including subcode component data which indicates ~~any~~ at least one of time information and information other than the time information, said circuit comprising:

a first generating portion for automatically generating the subcode component data which indicates the time information;

a second generating portion for automatically generating the subcode component data which indicates the information other than the time information;

a selecting portion which selects an output of at least one of the outputs of said first and second generating portions; and

a memory in which commands for automatic generation of the subcode component data are written,

wherein the commands include first commands for automatic generation of the subcode component data which indicates the time information, which first commands are written collectively in a first area of said memory, and second commands for automatic generation of the subcode component data which indicates the information other than the time information, which second commands are written collectively in a second area of said memory.

4. (Currently Amended) The subcode-data generating circuit, as claimed in claim 3, wherein:

said second generating portion comprises a plurality of generating portions provided separately;

said second area of said memory comprises a plurality of areas corresponding to said plurality of generating portions; and